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UNITED STATES PATENT APPLICATION

FOR

LOW INDUCTANCE CHIP WITH CENTER VIA CONTACT

BY

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TITLE: LOW INDUCTANCE CHIP WITH CENTER VIA CONTACT

BACKGROUND OF THE INVENTION

This invention generally relates to multi-layer ceramic capacitors (MLCs) adapted to be mounted to the surface of a circuit board. Further, the invention relates to a surface mount MLC device mounted on a circuit board and having a contact arrangement of alternating layers to achieve low inductance. More precisely, the present invention relates to a surface mount MLC device with a terminal arrangement providing low inductance for decoupling applications, such as high-speed microprocessor applications.

Advanced semiconductor circuits, particularly VLSI chips, almost universally employ decoupling capacitors. The decoupling capacitors are generally charged independent of circuit operation and are discharged to deliver a current that enables fast transition circuit switching with minimum noise. Closer physical location of the capacitor to the circuit allows for and is essential for higher switching speeds of the chip. If utilized in this manner, not only is the capacitance of the component important, but additionally, its inductance is crucial to overall performance.

In decoupling today's high speed digital circuits the capacitor is primarily being used to eliminate high-speed transient noise which is above its resonance point. In these applications it is desirable to maintain as low an

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inductance as possible. When a capacitor is mounted on a board, lead lengths and board lines are a major source of inductance. This inductance must be minimized to obtain good decoupling performance under high-speed transient conditions. The use of multiple capacitors instead of a few large bulk capacitors can be used to reduce inductance and gain more efficient surge-current availability.

While a large number of prior art capacitive devices are known, none is believed to be directly pertinent to low inductance surface mount MLC devices for decoupling applications, such as high-speed microprocessing. Prior art discoidal capacitors with through-holes are shown in references such as U.S. Patent Nos. 4,148,003, 5,177,633 and 4,247,881. While useful for their purpose, none of the prior art capacitive devices disclose or suggest a surface mount MLC in a generally square configuration for use in low inductance decoupling applications.

It is, therefore, desirable to provide an MLC, generally square-shaped, which exhibits low inductance and is capable of surface mounting on a circuit board for decoupling applications, such as high-speed microprocessing, with a first terminal around substantially the entire periphery of the device and a second opposing polarity terminal located by way of a through-via generally in the center of the device body.

SUMMARY OF THE INVENTION

The present invention recognizes and addresses various of the foregoing limitations and drawbacks, and others, concerning the lack of a surface mount multi-layer ceramic capacitor (MLC) device for low inductance decoupling applications. Therefore, the present invention provides a MLC device, generally square in configuration, for decoupling high frequency transients, in which the device has a first terminal substantially located around the entire periphery of the device and a second opposing polarity terminal located by way of a through-via in generally the middle of the device body.

It is, therefor, a principle object of the subject invention to provide an MLC device. More specifically, it is a object of the present device to provide an MLC device which exhibits a low inherent inductance. Most specifically, it is an object of the present invention to provide an MLC device with low inductance characteristics and a high capacitance/area which is readily adaptable to variation in size and dimension yet simple to manufacture and cost effective.

It is a further object of the present invention to provide a generally square-shaped MLC device. It is still a further object to provide a generally-square-shaped MLC device with a first terminal located substantially around the entire periphery of the device. It is still a further object of the present invention to provide a generally square-shaped MLC device with a first terminal located substantially around the entire periphery of the device and a second opposing polarity terminal located by way of a through-via in generally the middle of the

device body.

It is yet another object of the present invention to provide a single MLC device capable of making connection with numerous contacts located on the circuit board. It is still another object of the present invention to provide a multi-chip array comprised of a plurality of surface mount MLC devices in which the devices are arranged in a diamond pattern for high-speed microprocessor applications.

Additional objects and advantages of the invention are set forth in, or will be apparent to those of ordinary skill in the art from, the detailed description as follows. Also, it should be further appreciated that modifications and variations to the specifically illustrated and discussed features and materials hereof may be practiced in various embodiments and uses of this invention without departing from the spirit and scope thereof, by virtue of present reference thereto. Such variations may include, but are not limited to, substitutions of the equivalent means, features, and materials for those shown or discussed, and the functional or positional reversal of various parts, features, or the like.

Still further, it is to be understood that different embodiments, as well as different presently preferred embodiments, of this invention, may include various combinations or configurations of presently disclosed features, elements, or their equivalents (including combinations of features or configurations thereof not expressly shown in the figures or stated in the detailed description).

These and other features, aspects and advantages of the present invention will become better understood with reference to the following description and appended claims. The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate an embodiment of the invention and, together with the description, serve to explain the principles of the invention.

In one exemplary embodiment, a square "discoidal" capacitor device is provided having a ceramic body formed from a plurality of ceramic-electrode layers interleaved to form a stack. The stack is pressed and sintered to achieve a substantially unitary capacitor body. A first polarity terminal is located substantially about the entire periphery of the device body. A second polarity terminal is formed by a through-via located generally in the middle of the device body. The through-via may or may not be filled with solder.

In another exemplary embodiment, an array of surface mount MLC devices are mounted on a circuit board for use in low inductance decoupling applications, such as a high-speed microprocessor. The MLC devices are mounted in a diamond arrangement such that contacts of one polarity will be electrically connected to a first terminal located substantially about the entire periphery of the device body on each of such devices with direct electrical connection occurring at the corners of the device body. Contacts of an opposing polarity may be electrically connected to a through-via terminal located generally in the middle of each device body.

In a third embodiment of the present invention, a single surface mount MLC device is provided which makes electrical connection with a plurality of contact points on a circuit board. In this embodiment, all terminals of the device are formed by through-vias which align with respective contacts on the circuit board.

BRIEF DESCRIPTION OF THE DRAWINGS

A full and enabling disclosure of the present invention, including the best mode thereof, directed to one of ordinary skill in the art, is set forth in the specification, which makes reference to the appended figures, in which:

FIG. 1 is an isometric view of one embodiment of an MLC device constructed in accordance with the present invention;

FIG. 2 is a cross-section view of the embodiment of the present invention depicted in FIG. 1 showing the internal arrangement of the capacitor including the terminations;

FIGs. 3A and 3B are top views of alternating electrode layers which may be used to form the embodiment of the present invention as depicted in FIGs. 1 and 2;

FIG. 5 is an alternative embodiment of the present invention allowing the surface mounting of multiple MLCs for low inductance decoupling applications;

FIG. 6 is a second alternative embodiment of the present invention allowing for a single surface mount MLC to make connection with multiple

contacts on the circuit board; and

FIGs. 7A and 7B are top views of alternating electrode layers which may be used to form the embodiment of the present invention as depicted in FIG. 6.

Repeat use of reference characters throughout the present specification and appended drawings is intended to represent the same or analogous features or elements of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to presently preferred embodiments of the invention, examples of which are fully represented in the accompanying drawings. Such examples are provided by way of an explanation of the invention, not limitation thereof. In fact, it will be apparent to those skilled in the art that various modifications and variations can be made in the present invention, without departing from the spirit and scope thereof. For instance, features illustrated or described as part of one embodiment can be used on another embodiment to yield a still further embodiment. Still further, variations in selection of materials and/or characteristics may be practiced, to satisfy particular desired user criteria. Thus, it is intended that the present invention cover such modifications and variations as come within the scope of the present features and their equivalents.

As disclosed above, the present invention is particularly concerned with a multi-layer ceramic capacitive device for use in low inductance decoupling

applications, such as high-speed microprocessing. As shown in Figures 1 and 2, one preferred embodiment of the present invention is a generally square-shaped MLC device 10 formed from a plurality of parallel ceramic-electrode layers interleaved to form a stack. The stack may be pressed and sintered to achieve a substantially unitary capacitor body 12. A first polarity terminal 14 is located on all sides of the device body's periphery. A second polarity terminal 16 is formed by a through-via located generally in the middle of the device body 12. The second polarity terminal 16 may or may not be filled with solder (the via is filled with solder in the illustrated embodiment).

Figures 3A and 3B illustrate the two ceramic-electrode layers which are alternatively repeated and interleaved to produce the capacitor body 12. The first ceramic electrode-layer, as shown in Figure 3A, has a first electrode plate 18 covering substantially the entire underlying electrode sheet. A circular portion 20 of the sheet surrounding via 22 is left uncovered by first electrode plate 18 so as to prevent electrical connection between first electrode plate 18 and terminal 16. Instead, first electrode plate 18 is electrically connected to terminal 14 which extends substantially about the entire periphery of the device body 12.

As seen in Figure 3B, the second ceramic-electrode layer includes an second electrode plate 24 that extends to via 22 for making electrical connection with terminal 16. A perimeter region 26 of the ceramic sheet is left uncovered by second electrode plate 24 to prevent electrical connection between second

electrode plate 24 and terminal 14.

Figure 5 illustrates an alternative preferred embodiment of the present invention by which an array of surface mount MLC devices may be mounted for use in low inductance decoupling applications. Devices 10 may be mounted in a diamond arrangement such that contacts of one polarity may be electrically connected to terminal 16. Terminal 14 can make connection with four contacts of opposing polarity, one at each corner of the device body 12.

In a third preferred embodiment of the present invention, as seen in Figure 6, a single MLC capacitive device 28 may make connection with multiple contacts of the circuit board. In this third alternative preferred embodiment, all the terminals of the device 28 are formed by through-vias, which align with respective contacts on the circuit board.

Figures 7A and 7B illustrate the two types of ceramic-electrode layers which are alternatively repeated and interleaved to produce the capacitor body 12 of the third alternative preferred embodiment shown in Figure 6. The first ceramic electrode-layer, as shown in Figure 7A, has a first electrode plate 30 covering substantially the entire underlying electrode sheet. A circular portion 34 of the sheet surrounding through-via terminals 36 are left uncovered so as to prevent electrical connection between first electrode plate 30 and said through-via terminals 36. Instead, first electrode plate 30 is electrically connected to the alternative through-via terminals 38, all of an opposing polarity.

As seen in Figure 7B, the second ceramic-electrode layer includes an second electrode plate 32 covering substantially the entire underlying electrode sheet. A circular portion 34 of the sheet surrounding through-via terminals 38 are left uncovered so as to prevent electrical connection between second electrode plate 32 and said through-via terminals 38. Instead, second electrode plate 32 is electrically connected to the alternative through-via terminals 36.

Although a preferred embodiment of the invention has been described using specific terms and devices, such description is for illustrative purposes only. The words used are words of description rather than of limitation. It is to be understood that changes and variations may be made by those of ordinary skill in the art without departing from the spirit or the scope of the present invention, which is set forth in the following claims. In addition, it should be understood that aspects of various other embodiments may be interchanged both in whole or in part. Therefore, the spirit and scope of the appended claims should not be limited to the description of the preferred version contained herein.